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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,191	11/05/2001	Leonid B. Goldgeisser	005-1	7386

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,191	GOLDGEISSER ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 7/29/03 has been received and entered in the case.

2. The objections to the drawings in the last office action has been withdrawn based on applicant's drawings changes.

Claim Objections

3. Claims 1 and 7 are objected to because of the following informalities:

In claim 1, line 14, "elements, biasing" should be changed to --elements, said biasing--.

In claim 7, line 23, "elements, biasing" should be changed to --elements, said biasing--.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-7 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "the load and biasing elements" on line 15 are unclear antecedent basis, i.e., it is not clear which load element and which biasing element that the phrase refers to, i.e., the first element, the second load element or the first and second load elements, and the first biasing element, the second biasing element or the first and second biasing elements. Also, "a third stable operating point" on line 17 is also indefinite because it is insufficient antecedent basis for this limitation in the claim since there are no first and second stable operating points recited earlier.

Claims 2 and 3 are indefinite because they include the indefinite problem of claim 1.

In claim 4, "a third operating point" on line 20 is indefinite because it is insufficient antecedent basis for this limitation in the claim since there are no first and second operating points recited earlier.

Claims 5-6 are indefinite because they include the indefinite problem of claim 4.

In claim 7, line 7-8, the recitation "logic signals in either a first, second, or third state" is indefinite because it is not understood how a logic signal can have three states. It is known in the art that a logic signal has only two states such as logic Low and logic Hi. Clarification and/or appropriate correction is requested.

Also in claim 7, the recitation "the load and biasing elements" on line 24-25 and the recitation "a third stable operating point" are indefinite for the same reason as discussed in claim 1 above.

Also in claim 7, the recitation "a first input signal" on line 25-26 and "a second input signal" on line 38 are indefinite because it is not clear whether the first and second input signals are the same with the "ternary logic signals" recited on line 7 of the claim.

In claim 9, "one of three possible input signal levels" on line 2 is indefinite because it is not clear how a logic signal has three levels. It is known in the art that a logic signal has only two levels such as logic Low and logic Hi. Similarly, "logic input signal in a first, second or third state" is indefinite for the similar reason. Further, "the state" on line 10 and 12 is unclear antecedent basis since it is not know which state the phrase refers to. Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Dhong et al. (USP 4,816,706).

Insofar as understood in claim 1, Figure 9 of the Dhong et al. reference discloses a circuit which includes: a first series circuit (14, 48, 10, 18) coupling first (ground) and second (Vdd) supply voltage terminals (by way of transistors 24 and 22, respectively), with the first series circuit including a first load element (18) coupling the first supply voltage terminal (ground) to a first node (32), a first biasing element (48, 10) coupling the first node to a second node (26), and a first MOS transistor (14) coupling the second node to the second supply voltage terminal (Vdd); a second series circuit (20, 48, 12, 16) coupling the first (ground) and second (Vdd) supply voltage terminals (by way of transistors 24 and 22, respectively), with the second series circuit including a second load element (20) coupling the first supply voltage terminal to a third node (34), a second biasing element (48, 12) coupling the third node to a fourth node (28), and a second MOS transistor (16) coupling the fourth node to the second supply voltage terminal (Vdd); a feedback network (the connection of node 32 to gate of transistor 16, and the connection of node 34 to gate of transistor 14) coupling the first node (32) to the gate terminal of the second MOS transistor (16) and third node (34) to the gate terminal of the first MOS transistor (14); and wherein "said first and second load elements, biasing elements, and MOS transistors fabricate utilizing MOSFET technology and with the load and biasing elements

creating substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point" is also met because the structure of the claim is fully met (see In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977)).

With respect to claim 2, Figure 9 shows that each of the first (48,10) and second (48, 12) biasing elements includes a resistor (10 and 12. Note that it is known in the art that a p-channel MOS device having its gate connected to ground is a resistor, see p-channel transistor 22 in Figure 4 and Col. 6, lines 34-42 of Arcus – USP 6,124,741).

With respect to claim 3, Figure 9 shows that each of the first (48, 10) and second (48, 12) biasing elements includes a diode-connected transistor (48).

Insofar as understood in claim 9, Figure 9 of the Dhong et al. reference discloses a circuit as discussed with regard to claims 1-3 above. Hence, it also deemed to meet the limitations of the method recited in claim 9. Further, it is seen that the operating a latch circuit in a ternary logic unit is intended use (i.e., it is up to the designer to use the latch circuit in any environment such as in a memory unit or in a ternary unit, depends on the application).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over J. D. Heightley et al. (USP 3,540,010) in view of Wrathall et al. (USP 4,701,718).

With respect to claim 1, Figure 2 of the J. D. Heightley et al. reference discloses a circuit (19) which includes: a first series circuit (34, 28, 20) coupling first (V) and second (109) supply voltage terminals, with the first series circuit including a first load element (34) coupling the first supply voltage terminal (V) to a first node (32), a first biasing element (28) coupling the first node to a second node (collector of 20), and a first transistor (20) coupling the second node to the second supply voltage terminal (109); a second series circuit (35, 30, 21) coupling the first (V) and second (109) supply voltage terminals, with the second series circuit including a second load element (35) coupling the first supply voltage terminal to a third node (33), a second biasing element (30) coupling the third node to a fourth node (collector of 21), and a second transistor (21) coupling the fourth node to the second supply voltage terminal (109); a feedback network (the connection of the base of transistor 20 to node 33, and the connection of the base of transistor 21 to node 32). The different between the prior art and the claim invention is that the prior art reference fabricate the circuit using bipolar technology while the claim invention fabricate the circuit using MOSFET technology. However, the Wrathall et al. reference discloses that MOS technology offered some advantages over bipolar technology such as lower power and greater yield (Col. 1, lines 10-15). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the J. D. Heightley et al. reference to fabricate the circuit using MOS technology instead of bipolar technology for the purpose of improving the yield and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claim 1 including the first (20) and second (21) transistors are MOS transistors, and "with said first and second load elements, biasing elements, and MOS transistors fabricate utilizing MOSFET technology and with the load and biasing

elements creating substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point" is also met because the structure of the claim is fully met (see In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977)).

With respect to claim 2, Figure 2 of the J. D. Heightley et al. shows that each of the first (28) and second (30) biasing elements includes a resistor.

With respect to claim 9, the above combination et al. reference discloses a circuit as discussed with regard to claim 1 above. Hence, it also deemed to meet the limitations of the method recited in claim 9. Further, it is seen that the operating a latch circuit in a ternary logic unit is intended use (i.e., it is up to the designer to use the latch circuit in any environment such as in a memory unit or in a ternary unit, depends on the application).

10. Claims 1, 3, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waaben (USP 3,849,675) in view of Wrathall et al. (USP 4,701,718).

With respect to claim 1, Figure 1 of the Waaben reference discloses a circuit (10) which includes: a first series circuit (D18, D16, T12) coupling first (VD1) and second (Vref1) supply voltage terminals, with the first series circuit including a first load element (D18) coupling the first supply voltage terminal (VD1) to a first node (20), a first biasing element (D16) coupling the first node to a second node (collector of 12), and a first transistor (12) coupling the second node to the second supply voltage terminal (Vref1); a second series circuit (D24, D22, 14) coupling the first (VD1) and second (Vref1) supply voltage terminals, with the second series circuit including a second load element (D24) coupling the first supply voltage terminal to a third node (26), a second biasing element (D22) coupling the third node to a fourth node (collector of 14), and a second transistor (14) coupling the fourth node to the second supply voltage terminal

(Vref1); a feedback network (the connection of the base of transistor 12 to node 26, and the connection of the base of transistor 14 to node 20). The different between the prior art and the claim invention is that the prior art reference fabricate the circuit using bipolar technology while the claim invention fabricate the circuit using MOSFET technology. However, the Wrathall et al. reference discloses that MOS technology offered some advantages over bipolar technology such as lower power and greater yield (Col. 1, lines 10-15). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Waaben reference to fabricate the circuit using MOS technology instead of bipolar technology for the purpose of improving the yield and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claim 1 including the first (12) and second (14) transistors are MOS transistors, and "with said first and second load elements, biasing elements, and MOS transistors fabricate utilizing MOSFET technology and with the load and biasing elements creating substantially voltage drops to bias the MOS transistors in triode mode to achieve a third operating point" is also met because the structure of the claim is fully met (see In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977)).

With respect to claim 3, the above combination shows that each of the first (D16) and second (D22) biasing elements is a diode but does not specifically discloses that each of the biasing elements is a diode-connected transistor. However, it is well known in the art that a diode is easily formed from a transistor-connected (by connecting the gate of the transistor to the drain or source terminal of that transistor). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to use specific diode-connected transistor for broad diode for the purpose of easily integrated.

With respect to claim 9, the above combination et al. reference discloses a circuit as discussed with regard to claim 1 above. Hence, it also deemed to meet the limitations of the method recited in claim 9. Further, it is seen that the operating a latch circuit in a ternary logic unit is intended use (i.e., it is up to the designer to use the latch circuit in any environment such as in a memory unit or in a ternary unit, depends on the application).

11. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over J. D. Heightley et al. (USP 3,540,010) in view of Wrathall et al. (USP 4,701,718), and further in view of Arcus (USP 6,124,741).

With respect to claim 4, Figure 2 of the J. D. Heightley et al. reference discloses a circuit (19) which includes: a first series circuit (34, 28, 20) coupling first (V) and second (109) supply voltage terminals, with the first series circuit including a first load element (34) coupling the first supply voltage terminal (V) to a first node (32), a first biasing element (28) coupling the first node to a second node (collector of 20), and a first NPN transistor (20) coupling the second node to the second supply voltage terminal (109); a second series circuit (35, 30, 21) coupling the first (V) and second (109) supply voltage terminals, with the second series circuit including a second load element (35) coupling the first supply voltage terminal to a third node (33), a second biasing element (30) coupling the third node to a fourth node (collector of 21), and a second NPN transistor (21) coupling the fourth node to the second supply voltage terminal (109); a feedback network (the connection of the base of transistor 20 to node 33, and the connection of the base of transistor 21 to node 32). The different between the prior art and the claim invention is that the prior art reference fabricate the circuit using bipolar technology while the claim invention fabricate the circuit using MOSFET technology. However, the Wrathall et al. reference discloses

that MOS technology offered some advantages over bipolar technology such as lower power and greater yield (Col. 1, lines 10-15). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the J. D. Heightley et al. reference to fabricate the circuit using MOS technology instead of bipolar technology for the purpose of improving the yield and reducing the power consumption of the circuitry. Thus, in this combination, the first NPN transistor (20) and the second NPN transistor (21) are now n-channel MOSFET transistor.

The above combination meets all the limitation of claim 4 except that the first loading element is a first PMOS transistor and the second loading element is a second PMOS transistor. However, the Arcus reference (transistor 22 in Figure 4 and Col. 6, lines 34-42) discloses that a PMOS transistor that has its gate connected to ground is a resistor. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above combination to implement each of the resistor in the circuit by using a PMOS device having gate connected to ground because it functionally equivalent and easily integrated. Thus, this combinations meets all the limitation of claim 1 including the first PMOS (resistor 34 now is the first PMOS which having the gate connected to ground) and second PMOS (resistor 35 now is the second PMOS which having gate connected to ground) transistors, and "with said first and second load elements, biasing elements, and MOS transistors fabricate utilizing MOSFET technology and with the load and biasing elements creating substantially voltage drops to bias the MOS transistors in triode mode to achieve a third operating point" is also met because the structure of the claim is fully met (see In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977)).

Insofar as understood in claim 5, it is seen in the above combination (as discussed in claim 4) that each of the first (28) and second (30) biasing elements includes a resistor.

Allowable Subject Matter

12. Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 6 would be allowed because the prior art of record fails to disclose or suggest a tristable CMOS latch which includes a first series circuit having a first PMOS transistor, a first biasing element, and a first NMOS transistor; a second series circuit having a second PMOS transistor, a second biasing element, and a second NMOS transistor; and wherein the first biasing element is a diode-connected transistor and the second biasing element is a diode-connected transistor with the recited connections and operations set forth in this claim.

13. Claim 7 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claim 7 would be allowed because the prior art of record fails to disclose or suggest a MOS circuit which includes a current source; a first clocking transistor; a tristable MOS latch including a first series circuit having a first load element, a first biasing element and a first MOS transistor, and a second series circuit having a second load element, a second biasing element and a second MOS transistor; a second clock transistor; and an input circuit having first and second transistors with the recited connections and operations set forth in claim 7.

Response to Arguments

14. Applicant's arguments filed 7/29/03 have been fully considered but they are not persuasive.

Applicant argues that the Dhong reference does not disclose the functional limitation "the bias elements create substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point". This argument is not persuasive because the biasing elements of the Dhong reference are identical to each other so the biasing elements would create substantially identical voltage drop. Further, for broad reasonable interpretation, "a third stable operating point" is considered as just "a stable operating point" since there are no first and second stable operating points recited in the claims. Furthermore, assume there are first to third stable operating points recited in the claims, the Dhong reference also meets the functional limitation "the bias elements create substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point" because the structure of the claim is fully met (see In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977)).

Note that the similar reasoning also applied to the arguments with respect to other references in the rejection under 102 or 103.

Conclusion

15. Because the Examiner introduces a new rejection under 35 U.S.C. 112, 2nd paragraph, so this action is made non-final.

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

September 20, 2003

Long Nguyen
Art Unit: 2816